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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,295	09/10/2003	Daisuke Yoshida	00684.002964.1	2456

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,295	YOSHIDA, DAISUKE	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/505,194.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *27 December 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/505,194 (now Patent No. 6,670,938), filed on 16 February 2000.

Information Disclosure Statement

2. The information disclosure statement filed 27 December 2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. Although translated abstracts of the two listed foreign patent documents (JP 03-051887 and JP 08-305323) have been provided, no actual (Japanese language) copy of either foreign patent appears to have been submitted.

Specification

3. The disclosure is objected to because of the following informalities:

Page 5, Line 14 -- "Figure 2" should be changed to "Figure 20."

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 8-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiroki (US 6,628,253 B1).

Regarding claim 8, Hiroki discloses a liquid crystal apparatus, comprising: a liquid crystal device [Fig. 1; 101] comprising an active matrix substrate (see Column 1, Lines 8-12) having thereon a plurality of signal lines [Fig. 1; 103] arranged in columns, a plurality of scanning lines [Fig. 1; 102] arranged in rows, and pixel electrodes [Fig. 5A; A, B, C] each connected via a pixel switch [Fig. 5A; TFTs] to an intersection of the signal lines and the scanning lines so as to supply picture signals to the pixel electrodes via the signal lines, a counter substrate disposed opposite to the active matrix substrate, and a liquid crystal disposed between the active matrix substrate and the counter substrate (see Column 6, Line 63 - Column 7, Line 6), and drive means [Fig. 1; 105] for driving the liquid crystal device, wherein said drive means includes: a first common signal line [Fig. 2A; 129 output] and a second common signal line [Fig.

2A; 130 output] for supplying the picture signals to each of the plurality of signal lines, picture signal-supplying means [Fig. 2A; 129, 130] for supplying picture signals of one polarity [Fig. 4; 129] to the first common signal line and picture signals of the other polarity [Fig. 4; 130] to the second common signal line, first transfer switches [Fig. 2A; CMOS circuitry within the 'Sampling Circuit and Buffer Circuit' for odd numbered signal lines] each for connecting a respective column signal line with the first common signal line for selectively supplying one of the picture signals of one polarity to each column signal line, and second transfer switches [Fig. 2A; CMOS circuitry within the 'Sampling Circuit and Buffer Circuit' for even numbered signal lines] each for connecting a respective column signal line with the second common signal line for selectively supplying one of the picture signals of other polarity to each column signal line (see Column 8, Line 49 - Column 9, Line 19), and column inversion [Figs. 11A, 11B, 11C] drive means for: in a first frame [Fig. 4; '1 Frame'], selectively turning on the first transfer switches for odd-numbered column signal lines [Fig. 2A; 1, 3] and the second transfer switches for even-numbered column signal lines [Fig. 2A; 2, 4], and in a second frame [Fig. 4; 'Next Frame'], selectively turning on the second transfer switches for odd-numbered column signal lines [Fig. 2A; 1, 3] and the first transfer switches for even-numbered column signal lines [Fig. 2A; 2, 4] (see Column 11, Line 49 - Column 12, Line 9).

Regarding claim 9, this claim is rejected by the reasoning applied in rejecting claim 8; furthermore, Hiroki discloses a dot inversion [Fig. 12C] drive means for: in a first frame [Fig. 4; '1 Frame'], selectively turning on the first transfer switches for odd-numbered column signal lines [Fig. 2A; 1, 3] and the second transfer switches for even-numbered column signal lines

[Fig. 2A; 2, 4] at the time of scanning odd-numbered scanning lines [Fig. 2A; Scan Lines A & C], and selectively turning on the second transfer switches for odd-numbered column signal lines [Fig. 2A; 1, 3] and the first transfer switches for even-numbered column signal lines [Fig. 2A; 2, 4] at the time of scanning even-numbered scanning lines [Fig. 2A; Scan Lines B & D]; and in a second frame [Fig. 4; 'Next Frame'], selectively turning on the second transfer switches for odd-numbered column signal lines [Fig. 2A; 1, 3] and the first transfer switches for even-numbered column signal lines [Fig. 2A; 2, 4] at the time of scanning odd-numbered scanning lines [Fig. 2A; Scan Lines A & C], and selectively turning on the first transfer switches for odd-numbered column signal lines [Fig. 2A; 1, 3] and the second transfer switches for even-numbered column signal lines [Fig. 2A; 2, 4] at the time of scanning even-numbered scanning lines [Fig. 2A; Scan Lines B & D] (see Column 12, Lines 31-67).

Regarding claim 10, Hiroki discloses the first transfer switches comprise a transistor of a first conductivity type and the second transfer switches comprise a transistor of a second conductivity type different from the first conductivity type (see Fig. 2A; Column 10, Lines 13-29 -- in particular, see the CMOS circuitry within the 'Sampling Circuit and Buffer Circuit').

Regarding claim 11, Hiroki discloses the picture signal supply means includes first [Fig. 2A; 129] and second [Fig. 2A; 130] picture signal-generating means for generating positive-polarity picture signals [Fig. 4; 129] and negative-polarity picture signals [Fig. 4; 130], respectively, supplied to the first and second common signal lines, respectively; the first picture signal generating means generate picture signals in a range between a highest voltage and a

central voltage supplied to the pixel electrodes (see Fig. 4; Column 11, Line 49 - Column 12, Line 9); the second picture signal-generating means generates picture signals in a range between the central voltage and a lowest voltage supplied to the pixel electrodes; the first and second picture signal-garnering means are operated at different supply voltages; the supply voltages for the first picture signal-generating means are set to be the highest voltage + α and the central voltage - α; and the supply voltages for the second picture signal-generating means are set to be the central voltage + α and the lowest voltage - α, wherein α denotes α voltage lowering margin due to an internal resistance in the picture signal-generating means (see Column 10, Line 34 - Column 11, Line 3).

Regarding claim 12, Hiroki discloses α is in the range of 0 volt to 1 volt (see Fig. 4; Column 10, Line 34 - Column 11, Line 3).

Regarding claim 13, Hiroki discloses the first and second transfer switches and the picture signal supply means are disposed on a common substrate with the active matrix substrate (see Column 8, Lines 8-16).

Regarding claim 14, Hiroki discloses the active matrix substrate comprises an insulating substrate (see Column 8, Lines 25-41).

Regarding claim 15, Hiroki discloses the active matrix substrate comprises a single crystal substrate (see Column 8, Lines 25-41).

Response to Arguments

7. Applicant's arguments filed 6 July 2006 have been fully considered but they are not persuasive. The applicants contend the cited prior art of Hiroki (US 6,628,253 B1) neglects disclosing, "*first transfer switches each for connecting each column signal line with the first common signal line so as to selectively supply one of the picture signals of one polarity to each column signal line, and second transfer switches each for connecting each column signal line with the second common signal line so as to selectively supply one of the picture signals of the other polarity to each column signal line*" (see Page 9 of the 'Response to Second Notice of Non-Compliant Amendment' filed 6 July 2006).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "*first transfer switches each for connecting* ***each*** *column signal line with the first common signal line* ***so as to*** *selectively* ***supply*** *one of the picture signals of one polarity to each column signal line, and second transfer switches each for connecting* ***each*** *column signal line with the second common signal line* ***so as to*** *selectively* ***supply*** *one of the picture signals of the other polarity to each column signal line*" -- with emphasis added by the examiner) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

To the matter of actual claimed subject matter, Hiroki does indeed disclose first transfer switches [Fig. 2A; CMOS circuitry within the 'Sampling Circuit and Buffer Circuit' for odd

numbered signal lines] each for connecting a respective column signal line [Fig. 2A; signal lines(1, 3, etc.)] with the first common signal line [Fig. 2A; first analog video signal 129 output] for selectively supplying one of the picture [Fig. 2B; display pattern A1, B1, C1, A3, B3, C3, etc.] signals of one polarity [see Fig. 4; '1 Frame'] to each column signal line, and second transfer switches [Fig. 2A; CMOS circuitry within the 'Sampling Circuit and Buffer Circuit' for even numbered signal lines] each for connecting a respective column signal line [Fig. 2A; signal lines(2, 4, etc.)] with the second common signal line [Fig. 2A; second analog video signal 130 output] for selectively supplying one of the picture [Fig. 2B; display pattern A2, B2, C2, A4, B4, C4, etc.] signals of other polarity [see Fig. 4; 'Next Frame'] to each column signal line (see Column 8, Line 49 - Column 9, Line 19).

By such reasoning, rejection of the claims is deemed proper, necessary, and thereby maintained at this time.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The applicant is hereby notified that the examiner's art unit has recently changed from Art Unit 2673 to Art Unit 2629, please direct all future correspondence accordingly. Thank you.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Piziali
13 September 2006

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